(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（A）　(11)特許出願公開番号
特開2002－93942
（P2002－93942A）
(43)公開日　平成14年３月29日(2002.3.29)

(51)Int.Cl.⁷	識別記号	ＦＩ	ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０１Ｌ　23/12	５０１	Ｈ０１Ｌ　23/12	５０１Ｂ
			５０１Ｐ
			５０１Ｓ
			５０１Ｔ

審査請求　未請求　請求項の数11　ＯＬ　（全７頁）

(21)出願番号　特願2000－279089(P2000－279089)

(22)出願日　平成12年９月14日(2000.9.14)

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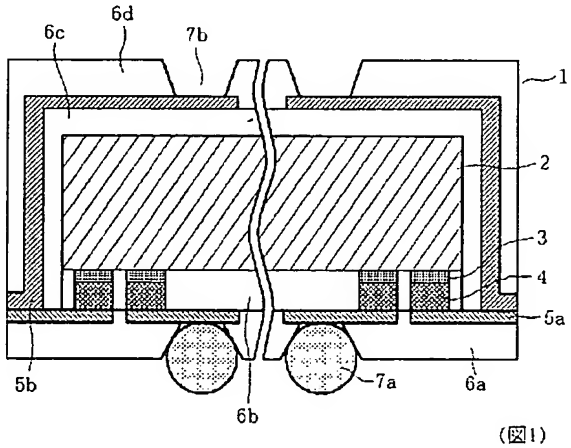
(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】　半導体装置の上下両面に外部端子を設けても、半導体装置の設計に制約を与えたり、半導体チップ面積の増加をもたらすことのないようにして、半導体装置の高密度実装の実現と、チップ面積の使用効率の向上を図る。
【解決手段】　半導体チップ２の能動素子面にはＡｌ製の電極３が形成され、電極３はバンプ４を介して導体５ａに接続されている。一部の導体５ａには外部端子７ａとして半田ボールが接続され、他の導体５ａはチップの側面から上面（裏面）上に延びる導体５ｂに接続されている。導体５ｂの一部の領域は外部端子７ｂになされている。半導体チップ２と導体５ａの間には絶縁体６ｂが充填され、半導体チップの側面と上面は絶縁体６ｃにより覆われ、半導体装置１の全体は外部端子形成領域を除いて絶縁体６ａ、６ｄに覆われている。



(図1)

1 半導体装置
2 半導体チップ
3 電極
4 バンプ
5a、5b 導体
6a、6b、6c、6d 絶縁体
7a、7b 外部端子

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【特許請求の範囲】

【請求項1】　半導体チップの第1の主面に半導体チップの金属電極に連なる配線を含む再配線層が形成され、前記第1の主面上の前記再配線層上に第1の外部端子が形成され、前記第1の主面の反対側の面である第2の主面上に前記再配線層に接続された第2の外部端子が形成されている半導体装置において、第2の外部端子はチップの側面に形成された側面配線を介して前記再配線層と接続され、かつ、前記側面配線の第1の主面側端部は“L”字状に曲げられその曲げられた部分が前記再配線層の前記第2の主面側の面と接触していることを特徴とする半導体装置。

【請求項2】　前記第1、第2の外部端子のうち少なくとも一方は導電性ボールにより構成されていることを特徴とする請求項1記載の半導体装置。

【請求項3】　少なくとも一部の外部端子は、配線層上を覆う絶縁膜が選択的に除去された配線部分によって構成されていることを特徴とする請求項1または2記載の半導体装置。

【請求項4】　前記側面配線にも外部端子が形成されていることを特徴とする請求項1記載の半導体装置。

【請求項5】　一部の再配線層の一端は第1の外部端子に接続され、その他端は前記側面配線を介して第2の外部端子と接続されていることを特徴とする請求項1記載の半導体装置。

【請求項6】　半導体チップの第1の主面に半導体チップの金属電極に連なる配線を含む再配線層が形成され、前記第1の主面上の前記再配線層上に第1の外部端子が形成されている半導体装置において、前記半導体チップの側面には前記再配線層の一部に接続された側面配線が形成されており、該側面配線には外部端子が形成されていることを特徴とする半導体装置。

【請求項7】　（1）第1の主面上に金属電極に連なる配線を含む再配線層が形成されているウェハを、前記再配線層の裏面が露出するように切断して溝を形成する工程と、（2）切断により形成された溝に絶縁体を埋め込む工程と、（3）埋め込まれた絶縁体の所定の箇所に前記再配線層の裏面を露出させるスルーホールを形成する工程と、（4）一端が前記再配線層に接続された、前記スルーホールの内壁面を覆う側面配線と、一端が前記側面配線に接続された、ウェハの第2の主面上に延在する第2主面配線層とを形成する工程と、（5）前記第（1）の工程における切断線に沿って切断を行い個々のチップに切り分ける工程と、を有することを特徴とする半導体装置の製造方法。

【請求項8】　前記第（4）の工程の後、前記第（5）の工程に先立って、外部端子形成領域上を除く前記第2主面配線上を覆い、かつ、前記スルーホール内を充填する絶縁体を形成する工程が付加されることを特徴とする請求項7記載の半導体装置の製造方法。

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【請求項9】　前記第（1）の工程の切断がダイサーにより行われることを特徴とする請求項7記載の半導体装置の製造方法。

【請求項10】　前記第（3）の工程において、スルーホールがレーザ光を用いて開口されることを特徴とする請求項7記載の半導体装置の製造方法。

【請求項11】　前記第（4）の工程において、　配線層がメッキ法により形成されることを特徴とする請求項7記載の半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置およびその製造方法に関し、さらに詳しくは、半導体チップの上下両面に外部端子を有する半導体装置およびその製造方法に関するものである。

【0002】

【従来の技術】近年、電子装置やシステムの小型化、高速化への要求は一段と高まってきており、これに応えるために実装技術面では、CSP(chip size package)からウェハ段階でパッケージングを行なうウェハレベルCSP技術が重要視されてきている。これとともにチップを積層してより高密度な実装を可能にする3次元実装技術が実現してきている。このような3次元実装を実現するためには、チップの表裏両面に外部端子を設けることが必要となる。

【0003】図6は、ウェハレベルCSP技術により作製された、チップの表裏両面に外部端子を有する従来の半導体装置21（以下、第1の従来例という）の断面図である。図6に示すように、半導体チップ22の能動素子面にはAlなどからなる電極23が形成されており、そのチップ表面はバンプ形成領域上を除いて絶縁体26bにより覆われている。一部の電極23はバンプ24を介して絶縁体26b上に形成された導体25aに接続されている。絶縁体26b上および導体25a上は、外部端子形成領域を除いて絶縁体26aにより覆われている。絶縁体26aの形成されていない領域には導体25aが露出しており、そこに外部端子27aが固着されている。電極23の一部は、基板を貫通して形成されたビアプラグ20を介してチップ裏面に形成された導体25bと接続されている。半導体チップ上および導体25b上は、外部端子27bとなる領域を除いて絶縁体26cにより被覆されている。しかしこの第1の従来例では、ビアプラグを形成するために半導体チップ22にスルーホールを開口する必要があり、そのスルーホールの開口位置によって素子配置や配線の引き回し制限を受けるため半導体装置の設計に制約を受けることがあった。また、スルーホールの面積分、半導体チップ面積が大きくなってしまうという問題点もあった。

【0004】一方、特開2000-91496号公報には、チップ側面に形成された導電膜（接続部）を介して

チップ表・裏面に形成された配線を接続する技術が提案されている。図7は、同公報にて開示された半導体装置（以下、第2の従来例という）の断面図である。同図に示されるように、CSP30のシリコン基板31の上面に形成された配線32、33は、シリコン基板31の側面に形成された接続部34およびシリコン基板31の下面に形成された配線35を介して柱状電極36に接続されている。そして、CSP30は、配線基板37上に異方導電性接着剤38を介して搭載され、CSP30上にはベアチップ39が搭載される。

【0005】

【発明が解決しようとする課題】上述した第1の従来例は、設計の自由度が制約を受け、またスルーホールによってチップ面積が消費されることによりチップ面積が増大してしまうという問題点があった。一方、第2の従来例では、チップ表・裏面を接続する接続部34と配線35との接触部が配線35の側面のみに限定されているため、接続が不安定になったり接触抵抗が高くなったりする欠点がある。本発明の課題は、上述した従来技術の問題点を解決することであって、その目的は、設計の自由度を制約することなくかつチップ面積を増大させることなくチップ表・裏面間を接続することができるようにするとともに、チップ表・裏面間を低抵抗でかつ信頼性高く接続できるようにすることである。

【0006】

【課題を解決するための手段】上記の目的を達成するため、本発明によれば、半導体チップの第1の主面に金属電極に連なる配線を含む再配線層が形成され、前記第1の主面上の前記再配線層上に第1の外部端子が形成され、前記第1の主面の反対側の面である第2の主面上に前記再配線層に接続された第2の外部端子が形成されている半導体装置において、第2の外部端子はチップの側面に形成された側面配線を介して前記再配線層と接続され、かつ、前記側面配線の第1の主面側端部は“L”字状に曲げられその曲げられた部分が前記再配線層の裏面と接触していることを特徴とする半導体装置、が提供される。

【0007】また、上記の目的を達成するため、本発明によれば、（1）第1の主面上に金属電極に連なる配線を含む再配線層が形成されているウェハを、前記再配線層の裏面が露出するように切断して溝を形成する工程と、（2）切断により形成された溝に絶縁体を埋め込む工程と、（3）埋め込まれた絶縁体の所定の箇所に前記再配線層の裏面を露出させるスルーホールを形成する工程と、（4）一端が前記再配線層に接続された前記スルーホールの内壁面を覆う側面配線と、一端が前記側面配線に接続された、ウェハの第2の主面上に延在する第2主面配線層とを形成する工程と、（5）前記第（1）の工程における切断線に沿って切断を行い個々のチップに切り分ける工程と、を有することを特徴とする半導体装置の製造方法、が提供される。

【0008】そして、好ましくは、前記第（4）の工程の後、前記第（5）の工程に先立って、外部端子形成領域上を除く前記第2主面配線上を覆い、かつ、前記スルーホール内を充填する絶縁体を形成する工程が付加される。また、好ましくは、前記第（1）の工程の切断がダイサーにより行われる。さらに、好ましくは、前記第（3）の工程において、スルーホールがレーザ光を用いて開口される。また、一層好ましくは、前記第（4）の工程において、配線層がメッキ法により形成される。

【0009】

【発明の実施の形態】次に、図面を参照して本発明の実施の形態について実施例に即して説明する。図1は、本発明の第1の実施例の半導体装置1の断面図である。半導体チップ2にはシリコンを用い、寸法が10×10×t0.3mmである。そして半導体チップ2の能動素子面（下面）上には、0.1×0.1mmの寸法でAl製の電極3がチップの周辺に沿って300個配列されている。電極3は、バンプ4を介して導体5aに電気的に接続されている。一部の導体5aの先端部には外部端子7aが固着され、他の一部の導体は、チップ側面からチップ上面へ延びる導体5bへ接続されている。導体5bの一部の領域は外部端子7bとなっている。

【0010】バンプ4はAu、導体5a、導体5bはCuを用いて形成した。バンプ4の厚さは50μm、導体5a、導体5bの膜厚は20μmとした。外部端子7aにはボール径250μmのPbSn（鉛・スズ）半田を用いたが、他の半田や表面に導電性膜の形成された絶縁性球等を用いてもよい。また、外部端子7bのようになにもなくてもよい。また、半導体チップ2と導体5aの間には、図示の省略された、電極3上に開口を有するパッシベーション膜と絶縁体6bとが形成されている。半導体チップの側面と上面は絶縁体6cによって被覆され、また、半導体装置1全体は、外部端子形成領域上に開口を有する絶縁体6a、6dにより被覆されている。絶縁体6a、6dは、ソルダーレジストで50μm厚、絶縁体6cは、エポキシ樹脂でチップ上面での膜厚は20μmである。また、絶縁体6bは、ポリイミド等の低弾性樹脂により形成されている。これら絶縁体のうち6aと6dは必ずしも必要ではないが、信頼性上形成することが好ましい。

【0011】本発明の半導体装置の特徴は、半導体装置の上下両面に電極を有することと、そのための配線を半導体チップ側面に有することと、その側面配線（導体5b）と再配線層（導体5a）との接続が平面上の接触によって達成されていることである。このように電気的接続が平面的な接触によって達成される配線が側面にあることにより、電気的な接続の信頼性を損ねることなく半導体チップは従来通り制約されることなく設計することができる。またさらに本実施例のように外部端子7aに

半田ボールを形成し、他の半導体装置の外部端子７ｂと接続することにより、この半導体装置は容易に何段でも重ねることができる。

【００１２】図２～図４は、本発明の第１の実施例の製造方法を工程順に示す断面図である。まず、Ａｌ製の電極３を有し、電極３上に開口を有するパッシベーション膜である絶縁体６ｅによって覆われたウェハ８上に、スパッタ法によりバリアメタルとなるＴｉ／ＴｉＮを堆積し、その上にＡｕを堆積してメッキ下地層４ａを形成する〔図２（ａ）〕。次に、フォトリソグラフィ法により、半導体ウェハ上のパッシベーション膜（絶縁体６ｅ）と同一パターンの開口を有するメッキレジスト膜１２を形成する〔図２（ｂ）〕。次に、電解メッキ法によりＡｕを５０μｍ程度堆積してバンプ４を形成し、その後メッキレジスト膜１２を剥離除去する〔図２（ｃ）〕。

【００１３】次に、そのバンプ４をマスクとして、不要なメッキ下地層３ａをエッチング除去し、その後、全面に絶縁体６ｂを堆積する。なお、以降の表示では、メッキ下地層４ａはバンプ４に含めて示し、絶縁体６ｅは絶縁体６ｂに含めて示すこととする〔図２（ｄ）〕。次に、その絶縁体６ｂをＣＭＰ法によりバンプ４の表面が露出するまで研磨し平坦化する。さらにその上にメッキレジスト膜１３を形成した後、メッキ活性化処理を行って全面に触媒層を形成し、メッキレジスト膜１３上の触媒層のみを除去する。そして無電解メッキ法によりＣｕを２０μｍ堆積して導体５ａを形成する。以上により再配線層１１が形成される〔図２（ｅ）〕。次に、メッキレジスト膜１３を剥離除去して、その全面にソルダーレジストを５０μｍ堆積して絶縁体６ａを形成し、その上にレジストマスク１４をパターニングする〔図２（ｆ）〕。

【００１４】次に、レジストマスク１４をマスクとして外部電極形成領域上の絶縁体６ａをドライエッチングにより除去する〔図３（ｇ）〕。なお、この絶縁体６ａのエッチングの工程は、後の図４（ｌ）の工程の際に行うようにしてもよい。次に、これを半導体チップ２に切断するため溝９を形成する。切断深さは、再配線層１１の導体５ａの手前、完全に絶縁体６ｂがなくなるところまでとした。切断にはダイシング装置を用い、その条件は、ブレード厚３００μｍ、切断速度６０ｍｍ／秒、回転数３００００ｒｐｍとした。またこのとき平面方向の切断の位置決めには赤外線を用いた。赤外線はシリコンを透過する性質をもつため、半導体チップ表面のＡｌ認識マーク（図示せず）を画像処理して読み取り、位置決めした。

【００１５】切断の深さは、完全に絶縁体６ｂを無くし、かつ導体５ａは残す深さにコントロールする必要がある。深さ方向の誤差として考えられるのは、ダイシング装置の深さ方向の機械的精度、ブレードの摩耗、部材厚さばらつきである。装置の機械的精度は０．５μｍである。またブレードの摩耗は何ラインか切断したら途中でオフセットをかけるようにすればキャンセルできる。部材厚のばらつきは、切断するのが導体５ａの手前までなので、それより下側にある絶縁体６ａの厚さばらつきだけを考慮すればよい。今回は絶縁体６ａの１層のみであるため２μｍ程度に抑えられている。よってトータル２．５μｍ程度であり、これを見込んで切断を行っても導体５ａが２．５μｍ程度深く研削されるだけなので問題はない。再配線層が多層となった場合は、研削を行ったり、導体５ａの厚さを厚くする等の工夫が必要である〔図３（ｈ）〕。

【００１６】次に、切断されたウェハ８上面に適量のエポキシ樹脂を塗布しスキージングして溝９に埋め込み、ウェハ上面および溝９内に絶縁体６ｃを形成した。そして、１５０℃１時間の熱処理を行って絶縁体６ｃを硬化させる〔図３（ｉ）〕。次に、埋め込まれた絶縁体６ｃの所定の箇所にスルーホール１０を形成する。このスルーホール形成にはレーザを用いた。スルーホール１０は絶縁体６ｃのみに形成し、導体５ａを貫通してはならないが、絶縁体と導体では絶縁体の方が弱いレーザ出力で削ることが可能なため、レーザ照射条件の設定は容易である〔図３（ｊ）〕。

【００１７】次に、スパッタ法によりＴｉ／ＴｉＮとＣｕからなるメッキ下地層を形成し、導体形成領域上に開口を有するメッキレジスト膜を形成した後、電解メッキによりＣｕを堆積して、スルーホール１０内壁、底面および絶縁体６ｃ上に導体５ｂを形成する。これにより、電極３、バンプ４、導体５ａ、導体５ｂは電気的に接続される。次に、メッキレジスト膜を除去し、露出したメッキ下地層をエッチング除去する〔図４（ｋ）〕。次に、ソルダーレジストである絶縁体６ｄを形成し、選択的に開口して導体５ｂを露出して外部端子７ｂを形成する〔図４（ｌ）〕。その後、外部端子７ａを形成する。外部端子７ａにはボール径２５０μｍのＰｂＳｎ（鉛・スズ）半田を用いたが、他の半田を用いてもよい。また外部端子７ｂのようになにもなくてもよい〔図４（ｍ）〕。最後に、切断して半導体装置１を得る。切断にはダイシング装置を用いた。ダイシング条件は、ブレード厚５０μｍ、切断速度６０ｍｍ／秒、回転数３００００ｒｐｍとした〔図４（ｎ）〕。

【００１８】図５は、本発明の第２の実施例の半導体装置１の断面図である。図５において図１に示した実施例の部分と同等の部分には、同じ参照番号が付せられているので重複する説明は省略する。本実施例においては、半導体装置１の側面の導体５ｂに外部電極７ｃを設けたものである。これによりさらなる高密度実装が可能となる。また、この半導体装置１の製造方法は、図１の半導体装置１の製造方法と同じであり、図４（ｎ）に示す切断工程が完了した後、レーザ等により絶縁体６ｄの一部

を除去して外部電極７ｃを設けることにより得られる。

【００１９】以上述べたように本発明の半導体装置の製造方法の特徴は、ウェハ状態で再配線を行った後、側面の配線を形成するために、一度切断する〔図３（ｈ）〕にもかかわらずウェハ一括処理できる点にある。ウェハを切断しても再配線層が半導体チップを支持しているため、各工程での位置決めが容易である。また一括処理のため工数も低減できる。

【００２０】以上、本発明の好ましい実施例について説明したが、本発明はこれら実施例に限定されるものではなく、本発明の要旨を逸脱することのない範囲内において適宜の変更が可能なものである。例えば、バンプの形成方法を電解メッキ法で行ったが、ボンディング法、蒸着法あるいは転写法で形成してもよい。また、実施例では、同一の導体５ｂ上に外部端子７ｂと７ｃを形成していたが、外部端子７ｃの形成された導体５ｂには他の外部端子を形成しないようにしてもよい。また、実施例では、すべての外部端子は半導体チップの電極３と接続されているが、必要に応じて電極に接続されずに、導体５ａ、５ｂにより相互に接続された外部端子を設けてもよい。

【００２１】

【発明の効果】以上説明したように、本発明の半導体装置は、半導体装置の上下両面に外部端子を配し、そのための側面配線の再配線層との接続部を平面的な接触により実現したものであるので、電気的な接続の信頼性を損ねることなく、チップ面積の有効利用を図るとともに半導体チップの設計の自由度を確保することができる。また、本発明の半導体装置の製造方法は、再配線層を切断することなくウェハを切断するようにしたものであるので、ウェハを切断してもウェハ状態を維持したまま、ウェハ一括処理でチップ側面の配線の形成と外部端子を形成を行うことができ、製造時のハンドリングが容易となり、また各工程での位置決めも容易となって、その結果製造工数の低減を図ることができる。

【図面の簡単な説明】

【図１】　本発明の第１の実施例の半導体装置の断面図。

【図２】　本発明の第１の実施例の半導体装置の製造方法を示す工程順の断面図（その１）。

【図３】　本発明の第１の実施例の半導体装置の製造方法を示す工程順の断面図（その２）。

【図４】　本発明の第１の実施例の半導体装置の製造方法を示す工程順の断面図（その３）。

【図５】　本発明の第２の実施例の半導体装置の断面図。

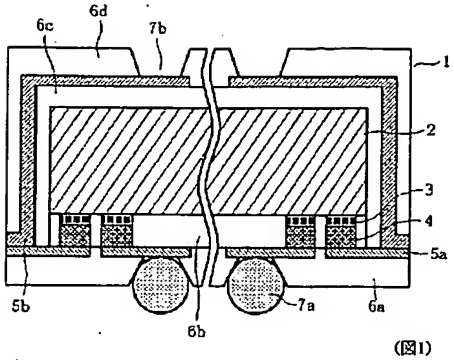
【図６】　第１の従来例の半導体装置の断面図。

【図７】　第２の従来例の半導体装置の断面図。

【符号の説明】

１、２１　半導体装置
２、２２　半導体チップ
３、２３　電極
４、２４　バンプ
４ａ　メッキ下地層
５ａ、５ｂ、２５ａ、２５ｂ　導体
６ａ、６ｂ、６ｃ、６ｄ、６ｅ、２６ａ、２６ｂ、２６ｃ　絶縁体
７ａ、７ｂ、７ｃ、２７ａ、２７ｂ　外部端子
８　ウェハ
９　溝
１０　スルーホール
１１　再配線層
１２、１３　メッキレジスト膜
１４　レジストマスク
２０　ビアプラグ
３０　ＣＳＰ
３１　シリコン基板
３２、３３、３５　配線
３４　接続部
３６　柱状電極
３７　配線基板
３８　異方導電性接着剤
３９　ベアチップ

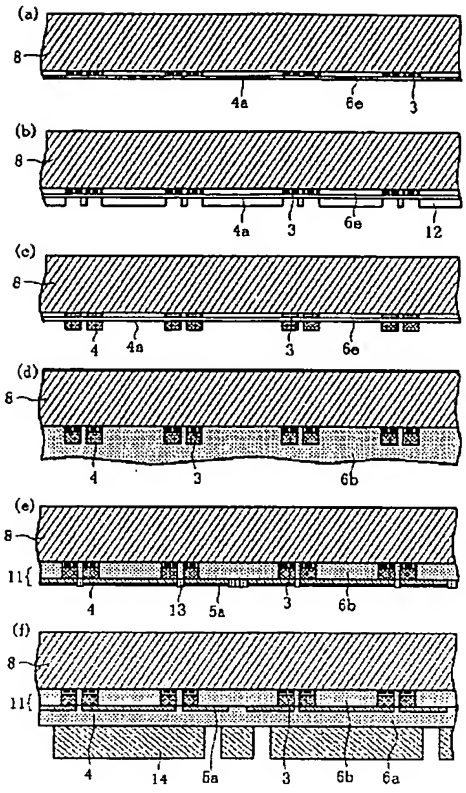
【図1】



(図1)

1 半導体装置
2 半導体チップ
3 電極
4 バンプ
5a、5b 導体
6a、6b、6c、6d 絶縁体
7a、7b 外部端子

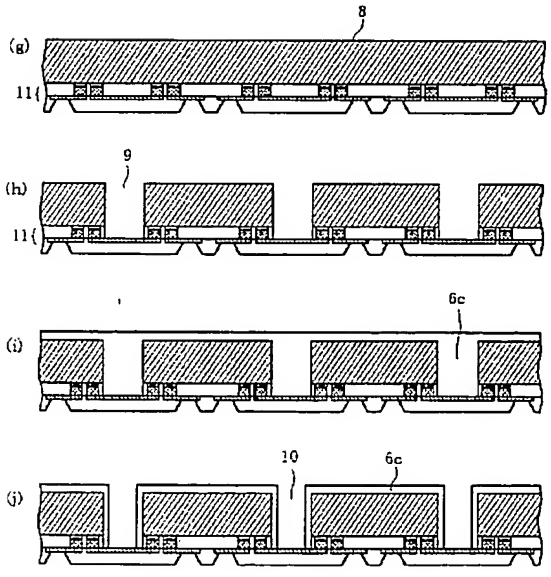
【図2】



4a メッキ下地層
6e 絶縁体
8 ウェハ
11 再配線層
12、13 メッキレジスト層
14 レジストマスク

(図2)

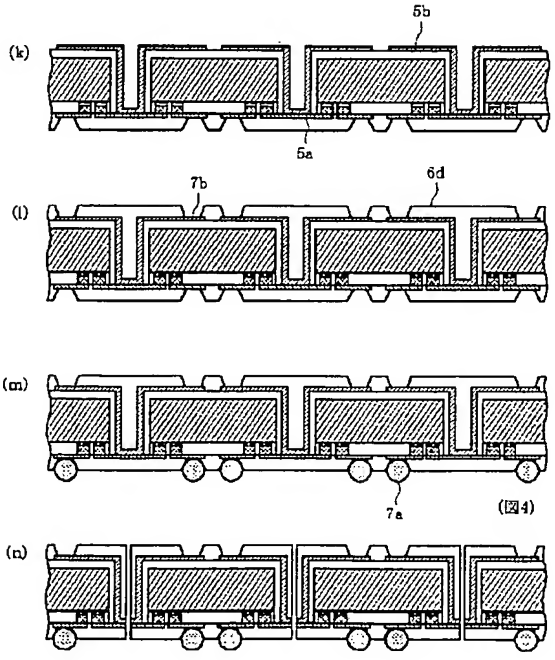
【図3】



9 梅
10 スルーホール

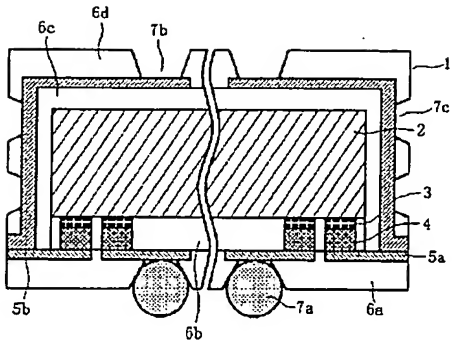
(図3)

【図4】



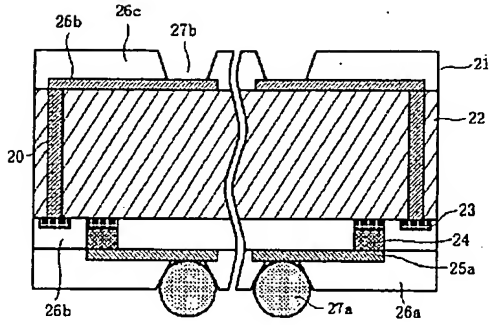
(図4)

【図5】



7c 外部端子　　(図5)

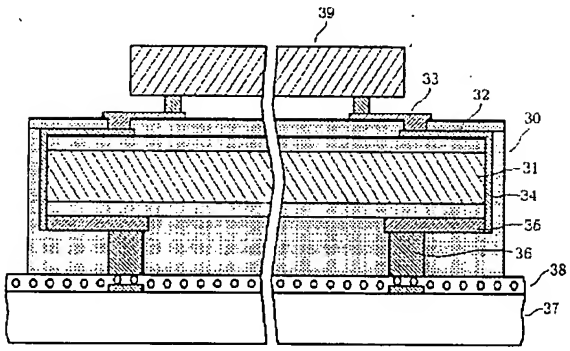
【図6】



(図6)

20 ビアプラグ
21 半導体装置
22 半導体チップ
23 電極
24 バンプ
25a、25b 導体
26a、26b、26c 絶縁体
27a、27b 外部端子

【図7】



30 CSP
31 シリコン基板
32、33、35 配線
34 接続部
36 柱状電極
37 配線基板
38 異方導電性接着剤
39 ベアチップ

(図7)

PAT-NO: JP02002093942A

DOCUMENT-IDENTIFIER: JP 2002093942 A

TITLE: SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUBN-DATE: March 29, 2002

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COUNTRY
N/A

APPL-NO: JP2000279089

APPL-DATE: September 14, 2000

INT-CL (IPC): H01L023/12

ABSTRACT:

PROBLEM TO BE SOLVED: To achieve the high-density packaging of a semiconductor device, and to improve the use efficiency of the area of a chip by preventing the design of the semiconductor device from being restricted, and by preventing the area of the semiconductor chip from being increased even if an external terminal is provided on both the upper and lower surfaces of the semiconductor device.

SOLUTION: On the surface of the active element of the semiconductor chip 2, an electrode 3 made of Al is formed, and is connected to a conductor 5a via a bump 4. One portion of the conductor 5a is connected to a soldering ball as an external terminal 7a, and the other is connected to a conductor 5b extended

from the side to upper surface (back surface) of the chip. The partial region
of the conductor 5b is set to an external terminal 7b. An insulator 6b is
filled between the semiconductor chip 2 and conductor 5b, the side and upper
surface of the semiconductor chip are covered with an insulator 6c, and the
entire semiconductor 1 other than an external terminal formation region is
covered with insulators 6a and 6d.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-093942

(43)Date of publication of application : 29.03.2002

(51)Int.Cl. H01L 23/12

(21)Application number : 2000-279089

(22)Date of filing : 14.09.2000

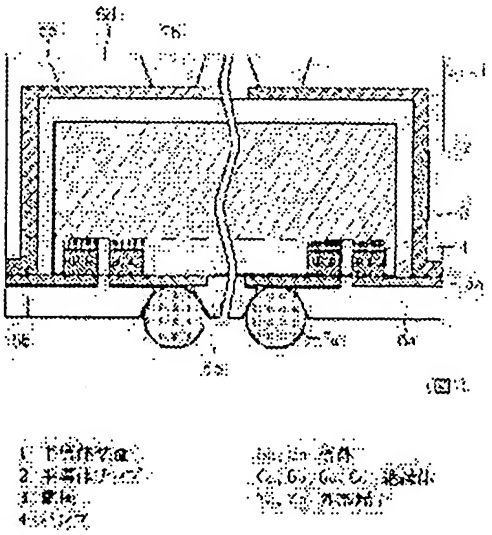
(71)Applicant : NEC CORP

(72)Inventor : KIMURA TAKEHIRO

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To achieve the high-density packaging of a semiconductor device, and to improve the use efficiency of the area of a chip by preventing the design of the semiconductor device from being restricted, and by preventing the area of the semiconductor chip from being increased even if an external terminal is provided on both the upper and lower surfaces of the semiconductor device.



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LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

JAPANESE [JP,2002-093942,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

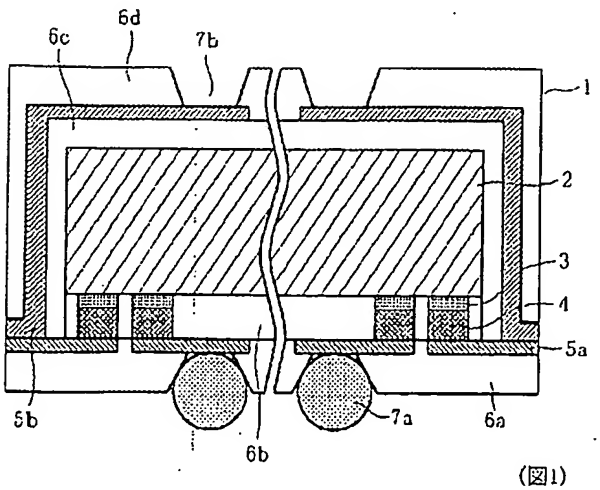
CLAIMS

[Claim(s)]
[Claim 1] The rewiring layer which includes wiring which stands in a row in the metal electrode of a semiconductor chip in the 1st principal plane of a semiconductor chip is formed. In the semiconductor device with which the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and the 2nd external terminal connected to said rewiring layer is formed on the 2nd principal plane which is the field of the opposite side of said 1st principal plane It is the semiconductor device characterized by connecting the 2nd external terminal with said rewiring layer through side-face wiring formed in the side face of a chip, and bending the 1st principal plane side edge section of said side-face wiring in the shape of an "L" character, and the bent part touching the field by the side of the 2nd [of said rewiring layer / said] principal plane.
[Claim 2] It is the semiconductor device according to claim 1 characterized by constituting at least one side with the conductive ball among the said 1st and 2nd external terminal.
[Claim 3] Some [at least] external terminals are semiconductor devices according to claim 1 or 2 characterized by being constituted by the wiring part from which the wrap insulator layer was alternatively removed in the wiring layer top.
[Claim 4] The semiconductor device according to claim 1 characterized by forming the external terminal also in said side-face wiring.
[Claim 5] It is the semiconductor device according to claim 1 characterized by connecting the end of some rewiring layers to the 1st external terminal, and connecting the other end with the 2nd external terminal through said side-face wiring.
[Claim 6] The semiconductor device characterized by forming in the side face of said semiconductor chip side-face wiring connected to said a part of rewiring layer in the semiconductor device with which the rewiring layer which includes wiring which stands in a row in the metal electrode of a semiconductor chip in the 1st principal plane of a semiconductor chip is formed, and the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and forming the external terminal in this side-face wiring.
[Claim 7] (1) The process which cuts so that the rear face of said rewiring layer may expose the wafer with which the rewiring layer including wiring which stands in a row in a metal electrode is formed on the 1st principal plane, and forms a slot, (2) (3) With the process which embeds an insulator in the slot formed of cutting The process which forms the through hole to which the rear face of said rewiring layer is exposed in the predetermined part of the embedded insulator, (4) An end the internal surface of said through hole connected to said rewiring layer Wrap side-face wiring, the process in which an end forms the 2nd principal plane wiring layer which was connected to said side-face wiring, and which extends on the 2nd [of a wafer] principal plane, and (5) -- the manufacture approach of the semiconductor device characterized by having the process which cuts along with the cutting plane line in the process of said ** (1), and is carved into each chip.
[Claim 8] The manufacture approach of the semiconductor device according to claim 7 characterized by adding the process which forms the insulator which covers said 2nd principal plane wiring top except an

external terminal formation field top in advance of the process of said ** (5) after the process of said ** (4), and is filled up with the inside of said through hole.
[Claim 9] The manufacture approach of the semiconductor device according to claim 7 characterized by cutting of the process of said ** (1) being performed by the dicer.
[Claim 10] The manufacture approach of the semiconductor device according to claim 7 characterized by carrying out opening of the through hole using a laser beam in the process of said ** (3).
[Claim 11] In the process of said ** (4) The manufacture approach of the semiconductor device according to claim 7 characterized by forming a wiring layer by plating.

[Translation done.]

Drawing selection Representative drawing



(図1)

1 半導体装置
2 半導体チップ
3 電極
4 バンプ
5a、5b 導体
6a、6b、6c、6d 絶縁体
7a、7b 外部端子

[Translation done.]

JAPANESE [JP,2002-093942,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which has an external terminal to vertical both sides of a semiconductor chip, and its manufacture approach in more detail about a semiconductor device and its manufacture approach.
[0002]
[Description of the Prior Art] In recent years, the demand to the miniaturization of an electronic instrument or a system and improvement in the speed is increasing much more, and in order to respond to this, in respect of mounting technology, importance has been attached to the wafer level CSP technique of performing packaging in a wafer phase from CSP (chip size package). Three-dimension mounting technology which carries out the laminating of the chip and enables higher-density mounting with this is being realized. In order to realize such three-dimension mounting, it is necessary to prepare an external terminal in front flesh-side both sides of a chip.
[0003] Drawing 6 is the sectional view of the conventional semiconductor device 21 (henceforth the 1st conventional example) which has an external terminal to front flesh-side both sides of a chip produced by the wafer level CSP technique. As shown in drawing 6 , the electrode 23 which consists of aluminum etc. is formed in the active element side of a semiconductor chip 22, and the chip front face is covered with insulator 26b except for the bump formation field top. the conductor with which some electrodes 23 were formed on insulator 26b through the bump 24 -- it connects with 25a. an insulator 26b top and a conductor -- 25a top is covered with insulator 26a except for the external terminal formation field. the field in which insulator 26a is not formed -- a conductor -- 25a is exposed and external terminal 27a has fixed there. the conductor formed in the chip rear face through the beer plug 20 formed by some. electrodes 23 penetrating a substrate -- it connects with 25b. a semiconductor chip top and a conductor -- 25b top is covered with insulator 26c except for the field used as external terminal 27b. However, in this 1st conventional example, since it was necessary to carry out opening of the through hole to a semiconductor chip 22 in order to form a beer plug, and the opening location of that through hole received component arrangement and a leading-about limit of wiring, constraint might be received in the design of a semiconductor device. Moreover, there was also a trouble that the surface integral of a through hole and semiconductor chip area will become large.
[0004] On the other hand, the technique which connects wiring formed in the chip table and the rear face through the electric conduction film (connection) formed in the tip side side is proposed by JP,2000-91 496,A. Drawing 7 is the sectional view of the semiconductor device (henceforth the 2nd conventional example) indicated in this official report. As shown in this drawing, the wiring 32 and 33 formed in the top face of the silicon substrate 31 of CSP30 is connected to the pillar-shaped electrode 36 through the wiring 35 formed in the inferior surface of tongue of the connection 34 formed in the side face of a silicon substrate 31, and a silicon substrate 31. And CSP30 is carried through the different direction electroconductive glue 38 on the wiring substrate 37, and a bare chip 39 is carried on CSP30.
[0005]

[Problem(s) to be Solved by the Invention] The 1st conventional example mentioned above had the trouble that a chip area will increase, when the degree of freedom of a design received constraint and a chip area was consumed by the through hole. On the other hand, in the 2nd conventional example, since the contact section of the connection 34 and wiring 35 which connect a chip table and a rear face is limited only to the side face of wiring 35, there is a fault to which connection becomes unstable or contact resistance becomes high. while the technical problem of this invention is solving the trouble of the conventional technique mentioned above, and the purpose enables it to connect between a chip table and a rear face, without [without it restrains the degree of freedom of a design, and] increasing a chip area -- between a chip table and a rear face -- low resistance -- and dependability -- it is enabling it to connect highly.

[0006]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, according to this invention, the rewiring layer which includes wiring which stands in a row in a metal electrode in the 1st principal plane of a semiconductor chip is formed. In the semiconductor device with which the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and the 2nd external terminal connected to said rewiring layer is formed on the 2nd principal plane which is the field of the opposite side of said 1st principal plane The 2nd external terminal is connected with said rewiring layer through side-face wiring formed in the side face of a chip, and the 1st principal plane side edge section of said side-face wiring is bent in the shape of an "L" character, and semiconductor device ** to which the bent part is characterized by being in contact with the rear face of said rewiring layer is offered.

[0007] moreover -- according to [in order to attain the above-mentioned purpose] this invention -- (1) -- with the process which cuts so that the rear face of said rewiring layer may expose the wafer with which the rewiring layer including wiring which stands in a row in a metal electrode is formed on the 1st principal plane, and forms a slot (2) (3) With the process which embeds an insulator in the slot formed of cutting The process which forms the through hole to which the rear face of said rewiring layer is exposed in the predetermined part of the embedded insulator, (4) An end the internal surface of said through hole connected to said rewiring layer Wrap side-face wiring, The process in which an end forms the 2nd principal plane wiring layer which was connected to said side-face wiring, and which extends on the 2nd [of a wafer] principal plane, (5) Manufacture approach ** of the semiconductor device characterized by having the process which cuts along with the cutting plane line in the process of said ** (1), and is carved into each chip is offered.

[0008] And the process which forms the insulator which covers said 2nd principal plane wiring top except an external terminal formation field top in advance of the process of said ** (5) after the process of said ** (4), and is preferably filled up with the inside of said through hole is added. Moreover, cutting of the process of said ** (1) is preferably performed by the dicer. Furthermore, in the process of said ** (3), opening of the through hole is preferably carried out using a laser beam. Moreover, in the process of said ** (4), a wiring layer is formed by plating much more preferably.

[0009]

[Embodiment of the Invention] Next, with reference to a drawing, it is based on an example and the gestalt of operation of this invention is explained. Drawing 1 is the sectional view of the semiconductor device 1 of the 1st example of this invention. A dimension is 10x10xt0.3mm, using silicon in a semiconductor chip 2. And on the active element side (inferior surface of tongue) of a semiconductor chip 2, 300 electrodes 3 made from aluminum are arranged along the circumference of a chip with the dimension of 0.1x0.1mm. an electrode 3 -- a bump 4 -- minding -- a conductor -- it connects with 5a electrically. some conductors -- the conductor with which external terminal 7a fixes to the point of 5a, and some [other] conductors are prolonged from a tip side side to a chip top face -- it connects with 5b. Some fields which are conductor 5b are external terminal 7b.

[0010] a bump 4 -- Au, conductor 5a, and a conductor -- 5b was formed using Cu. a bump's 4 thickness -- 50 micrometers, conductor 5a, and a conductor -- the thickness of 5b could be 20 micrometers.

Although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a, the insulating ball with which the conductive film was formed in other solder and front

faces may be used. Moreover, nothing may not be like external terminal 7b. moreover, a semiconductor chip 2 and a conductor -- between 5a, the passivation film and insulator 6b to which illustration was abbreviated and which have opening on an electrode 3 are formed. The side face and top face of a semiconductor chip are covered with insulator 6c, and the semiconductor device 1 whole is covered with the insulators 6a and 6d which have opening on an external terminal formation field. Insulators 6a and 6d is [the thickness on the top face of a chip of 50 micrometer thickness and insulator 6c] 20 micrometers in an epoxy resin at a solder resist. Moreover, insulator 6b is formed with low elastic resin, such as polyimide. Although the inside 6a and 6d of these insulators is not necessarily required, forming on dependability is desirable.

[0011] The descriptions of the semiconductor device of this invention are to have an electrode to vertical both sides of a semiconductor device, to have wiring for it on a semiconductor chip side face, and that connection with the side-face wiring (conductor 5b) and rewiring layer (conductor 5a) is attained by contact on a flat surface. Thus, when a side face has wiring with which electrical installation is attained by superficial contact, a semiconductor chip can be designed, without being restrained as usual, without spoiling the dependability of electric connection. Furthermore, any number of steps of this semiconductor device can be easily piled up by forming a solder ball in external terminal 7a like this example, and connecting with external terminal 7b of other semiconductor devices.

[0012] Drawing 2 - drawing 4 are the sectional views showing the manufacture approach of the 1st example of this invention in order of a process. First, on the wafer 8 covered with insulator 6e which has the electrode 3 made from aluminum and has opening on an electrode 3, and which is the passivation film, Ti/TiN which serves as barrier metal by the spatter is deposited, Au is deposited on it and plating substrate layer 4a is formed [drawing 2 (a)]. Next, the plating resist film 12 which has opening of the same pattern as the passivation film on a semi-conductor wafer (insulator 6e) is formed by the photolithography method [drawing 2 (b)]. Next, about 50 micrometers of Au(s) are deposited with electrolysis plating, a bump 4 is formed, and exfoliation removal of the plating resist film 12 is carried out after that [drawing 2 (c)].

[0013] Next, etching removal of the unnecessary plating substrate layer 3a is carried out by using the bump 4 as a mask, and insulator 6b is deposited all over after that. In addition, suppose that plating substrate layer 4a is included and shown to a bump 4, and insulator 6e is included in insulator 6b, and it is shown in subsequent displays [drawing 2 (d)]. Next, flattening is ground and carried out until a bump's 4 front face exposes the insulator 6b by the CMP method. After forming the plating resist film 13 on it furthermore, plating activation is performed, a catalyst bed is formed in the whole surface, and only the catalyst bed on the plating resist film 13 is removed. and an electroless deposition method -- Cu -- 20 micrometers -- depositing -- a conductor -- 5a is formed. The rewiring layer 11 is formed of the above [drawing 2 (e)]. Next, exfoliation removal of the plating resist film 13 is carried out, 50 micrometers of solder resists are deposited all over the, insulator 6a is formed, and patterning of the resist mask 14 is carried out on it [drawing 2 (f)].

[0014] Next, dry etching removes insulator 6a on an external electrode formation field by using the resist mask 14 as a mask [drawing 3 (g)]. In addition, it may be made to perform the process of etching of this insulator 6a in the case of the process of next drawing 4 (l). Next, a slot 9 is formed in order to cut this to a semiconductor chip 2. the cutting depth -- the conductor of the rewiring layer 11 -- it carried out to to this side of 5a, and the place whose insulator 6b is lost completely. The condition was set to the blade thickness of 300 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm at cutting using dicing equipment. Moreover, infrared radiation was used for positioning of cutting of the direction of a flat surface at this time. Since infrared radiation had the property which penetrates silicon, it carried out the image processing of the aluminum recognition mark on the front face of a semiconductor chip (not shown), read it, and was positioned.

[0015] the depth of cutting -- perfect -- insulator 6b -- losing -- and a conductor -- it is necessary to control 5a in the depth to leave Wear of the mechanical precision of the depth direction of dicing equipment and a blade and member thickness dispersion are thought as an error of the depth direction. The mechanical precision of equipment is 0.5 micrometers. Moreover, if the wear of some lines of a

blade is cut and offset will be applied on the way, it is cancellable. cutting dispersion in member thickness -- a conductor -- what is necessary is to take into consideration only thickness dispersion of insulator 6a which is below it, since it is to this side of 5a Since it is only one layer of insulator 6this time, it is stopped by about 2 micrometers. Therefore, it is about total 2.5micrometer, and since grinding of the five ais only deeply carried out about 2.5 micrometers of conductors even if it cuts by expecting this, it is satisfactory. performing grinding, when a rewiring layer turns into a multilayer **** -- a conductor -- [drawing 3 (h)] which needs the device of thickening thickness of 5a.

[0016] Next, skiing JINGU of the epoxy resin of optimum dose was applied and carried out on the wafer 8 cut top face, it embedded in the slot 9, and insulator 6c was formed in the wafer top face and the slot 9. And 150-degree-C heat treatment of 1 hour is performed, and insulator 6c is stiffened [drawing 3 (i)]. Next, a through hole 10 is formed in the predetermined part of embedded insulator 6c. Laser was used for this through hole formation. a through hole 10 -- insulator 6c -- forming -- a conductor -- although 5a must not be penetrated, since it is possible to delete by the laser output with the weaker insulator in an insulator and a conductor -- [drawing 3 (j)] with an easy setup of laser radiation conditions.

[0017] next, the plating substrate layer which consists of Ti/TiN and Cu by the spatter -- forming -- a conductor -- the electrolytic plating after forming the plating resist film which has opening on a formation field -- Cu -- depositing -- a through hole 10 wall, base, and insulator 6c top -- a conductor -- 5b is formed. thereby -- an electrode 3, a bump 4, conductor 5a, and a conductor -- 5b is connected electrically. Next, the plating resist film is removed and etching removal of the exposed plating substrate layer is carried out [drawing 4 (k)]. 6d of next, insulators which are a solder resist -- forming -- alternative -- opening -- carrying out -- a conductor -- [drawing 4 (l)] which exposes 5b and forms external terminal 7b. Then, external terminal 7a is formed. Other solder may be used although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a. Moreover, nothing may not be like external terminal 7b [drawing 4 (m)]. . At the end, it cuts and a semiconductor device 1 is obtained. Dicing equipment was used for cutting. Dicing conditions were set to the blade thickness of 50 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm [drawing 4 (n)].

[0018] Drawing 5 is the sectional view of the semiconductor device 1 of the 2nd example of this invention. the same reference number should give a part equivalent to the part of the example shown in drawing 1 in drawing 5 -- the explanation which overlaps in that of ********** is omitted. this example -- setting -- the conductor of the side face of a semiconductor device 1 -- external electrode 7c is prepared in 5b. Thereby, the further high density assembly becomes possible. Moreover, the manufacture approach of this semiconductor device 1 is the same as the manufacture approach of the semiconductor device 1 of drawing 1 , and after the cutting process shown in drawing 4 (n) is completed, it is acquired by laser's etc. removing 6d of some insulators, and preparing external electrode 7c.

[0019] As stated above, the description of the manufacture approach of the semiconductor device of this invention is that it can carry out wafer batch processing in spite of [drawing 3 (h)] cut once, in order to form wiring of a side face, after performing rewiring in the state of a wafer. Since the rewiring layer is su pporting the semiconductor chip even if it cuts a wafer, positioning at each process is easy. Moreover, a man day can also be reduced for batch processing.

[0020] As mentioned above, although the desirable example of this invention was explained, proper modification is possible for this invention within limits which are not limited to these examples and do not deviate from the summary of this invention. For example, although a bump's formation approach was performed with electrolysis plating, you may form with the bonding method, vacuum deposition, or a replica method. moreover, the conductor same in the example -- although the external terminals 7b and 7c were formed on 5b, you may make it not form other external terminals in conductor 5b in which external terminal 7c was formed Moreover, in the example, all external terminals may prepare the external terminal mutually connected by Conductors 5a and 5b, without connecting with an electrode if needed, although it connects with the electrode 3 of a semiconductor chip.

[0021]

[Effect of the Invention] As explained above, the semiconductor device of this invention can secure the degree of freedom of a design of a semiconductor chip, without spoiling the dependability of electric connection, since an external terminal is arranged on vertical both sides of a semiconductor device and superficial contact realizes a connection with the rewiring layer of side-face wiring for it while aiming at a deployment of a chip area. Moreover, formation and the external terminal of wiring of a tip side side can be formed by wafer batch processing, and the handling at the time of manufacture becomes easy, maintaining a wafer condition, even if it cut the wafer, since the wafer was cut without cutting a rewiring layer, and positioning at each process also becomes easy, and, as a result, the manufacture approach of the semiconductor device of this invention can aim at reduction of a manufacture man day.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the semiconductor device which has an external terminal to vertical both sides of a semiconductor chip, and its manufacture approach in more detail about a semiconductor device and its manufacture approach.

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PRIOR ART

[Description of the Prior Art] In recent years, the demand to the miniaturization of an electronic instrument or a system and improvement in the speed is increasing much more, and in order to respond to this, in respect of mounting technology, importance has been attached to the wafer level CSP technique of performing packaging in a wafer phase from CSP (chip size package). Three-dimension mounting technology which carries out the laminating of the chip and enables higher-density mounting with this is being realized. In order to realize such three-dimension mounting, it is necessary to prepare an external terminal in front flesh-side both sides of a chip.
[0003] Drawing 6 is the sectional view of the conventional semiconductor device 21 (henceforth the 1st conventional example) which has an external terminal to front flesh-side both sides of a chip produced by the wafer level CSP technique. As shown in drawing 6 , the electrode 23 which consists of aluminum etc. is formed in the active element side of a semiconductor chip 22, and the chip front face is covered with insulator 26b except for the bump formation field top. the conductor with which some electrodes 23 were formed on insulator 26b through the bump 24 -- it connects with 25a. an insulator 26b top and a conductor -- 25a top is covered with insulator 26a except for the external terminal formation field. the field in which insulator 26a is not formed -- a conductor -- 25a is exposed and external terminal 27a has fixed there. the conductor formed in the chip rear face through the beer plug 20 formed by some electrodes 23 penetrating a substrate -- it connects with 25b. a semiconductor chip top and a conductor -- 25b top is covered with insulator 26c except for the field used as external terminal 27b. However, in this 1st conventional example, since it was necessary to carry out opening of the through hole to a semiconductor chip 22 in order to form a beer plug, and the opening location of that through hole received component arrangement and a leading-about limit of wiring, constraint might be received in the design of a semiconductor device. Moreover, there was also a trouble that the surface integral of a through hole and semiconductor chip area will become large.
[0004] On the other hand, the technique which connects wiring formed in the chip table and the rear face through the electric conduction film (connection) formed in the tip side side is proposed by JP,2000-91496,A. Drawing 7 is the sectional view of the semiconductor device (henceforth the 2nd conventional example) indicated in this official report. As shown in this drawing, the wiring 32 and 33 formed in the top face of the silicon substrate 31 of CSP30 is connected to the pillar-shaped electrode 36 through the wiring 35 formed in the inferior surface of tongue of the connection 34 formed in the side face of a silicon substrate 31, and a silicon substrate 31. And CSP30 is carried through the different direction electroconductive glue 38 on the wiring substrate 37, and a bare chip 39 is carried on CSP30.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, the semiconductor device of this invention can secure the degree of freedom of a design of a semiconductor chip, without spoiling the dependability of electric connection, since an external terminal is arranged on vertical both sides of a semiconductor device and superficial contact realizes a connection with the rewiring layer of side-face wiring for it while aiming at a deployment of a chip area. Moreover, formation and the external terminal of wiring of a tip side side can be formed by wafer batch processing, and the handling at the time of manufacture becomes easy, maintaining a wafer condition, even if it cut the wafer, since the wafer was cut without cutting a rewiring layer, and positioning at each process also becomes easy, and, as a result, the manufacture approach of the semiconductor device of this invention can aim at reduction of a manufacture man day.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The 1st conventional example mentioned above had the trouble that a chip area will increase, when the degree of freedom of a design received constraint and a chip area was consumed by the through hole. On the other hand, in the 2nd conventional example, since the contact section of the connection 34 and wiring 35 which connect a chip table and a rear face is limited only to the side face of wiring 35, there is a fault to which connection becomes unstable or contact resistance becomes high. while the technical problem of this invention is solving the trouble of the conventional technique mentioned above, and the purpose enables it to connect between a chip table and a rear face, without [without it restrains the degree of freedom of a design, and] increasing a chip area -- between a chip table and a rear face -- low resistance -- and dependability -- it is enabling it to connect highly.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to attain the above-mentioned purpose, according to this invention, the rewiring layer which includes wiring which stands in a row in a metal electrode in the 1st principal plane of a semiconductor chip is formed. In the semiconductor device with which the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and the 2nd external terminal connected to said rewiring layer is formed on the 2nd principal plane which is the field of the opposite side of said 1st principal plane The 2nd external terminal is connected with said rewiring layer through side-face wiring formed in the side face of a chip, and the 1st principal plane side edge section of said side-face wiring is bent in the shape of an "L" character, and semiconductor device ** to which the bent part is characterized by being in contact with the rear face of said rewiring layer is offered.
[0007] moreover -- according to [in order to attain the above-mentioned purpose] this invention -- (1) -- with the process which cuts so that the rear face of said rewiring layer may expose the wafer with which the rewiring layer including wiring which stands in a row in a metal electrode is formed on the 1st principal plane, and forms a slot (2) (3) With the process which embeds an insulator in the slot formed of cutting The process which forms the through hole to which the rear face of said rewiring layer is exposed in the predetermined part of the embedded insulator, (4) An end the internal surface of said through hole connected to said rewiring layer Wrap side-face wiring, The process in which an end forms the 2nd principal plane wiring layer which was connected to said side-face wiring, and which extends on the 2nd [of a wafer] principal plane, (5) Manufacture approach ** of the semiconductor device characterized by having the process which cuts along with the cutting plane line in the process of said ** (1), and is carved into each chip is offered.
[0008] And the process which forms the insulator which covers said 2nd principal plane wiring top except an external terminal formation field top in advance of the process of said ** (5) after the process of said ** (4), and is preferably filled up with the inside of said through hole is added. Moreover, cutting of the process of said ** (1) is preferably performed by the dicer. Furthermore, in the process of said ** (3), opening of the through hole is preferably carried out using a laser beam. Moreover, in the process of said ** (4), a wiring layer is formed by plating much more preferably.
[0009]
[Embodiment of the Invention] Next, with reference to a drawing, it is based on an example and the gestalt of operation of this invention is explained. Drawing 1 is the sectional view of the semiconductor device 1 of the 1st example of this invention. A dimension is 10x10xt0.3mm, using silicon in a semiconductor chip 2. And on the active element side (inferior surface of tongue) of a semiconductor chip 2, 300 electrodes 3 made from aluminum are arranged along the circumference of a chip with the dimension of 0.1x0.1mm. an electrode 3 -- a bump 4 -- minding -- a conductor -- it connects with 5a electrically. some conductors -- the conductor with which external terminal 7a fixes to the point of 5a, and some [other] conductors are prolonged from a tip side side to a chip top face -- it connects with 5b. Some fields which are conductor 5b are external terminal 7b.
[0010] a bump 4 -- Au, conductor 5a, and a conductor -- 5b was formed using Cu. a bump's 4 thickness -- 50 micrometers, conductor 5a, and a conductor -- the thickness of 5b could be 20 micrometers.

Although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a, the insulating ball with which the conductive film was formed in other solder and front faces may be used. Moreover, nothing may not be like external terminal 7b. moreover, a semiconductor chip 2 and a conductor -- between 5a, the passivation film and insulator 6b to which illustration was abbreviated and which have opening on an electrode 3 are formed. The side face and top face of a semiconductor chip are covered with insulator 6c, and the semiconductor device 1 whole is covered with the insulators 6a and 6d which have opening on an external terminal formation field. Insulators 6a and 6d is [the thickness on the top face of a chip of 50 micrometer thickness and insulator 6c] 20 micrometers in an epoxy resin at a solder resist. Moreover, insulator 6b is formed with low elastic resin, such as polyimide. Although the inside 6a and 6d of these insulators is not necessarily required, forming on dependability is desirable.

[0011] The descriptions of the semiconductor device of this invention are to have an electrode to vertical both sides of a semiconductor device, to have wiring for it on a semiconductor chip side face, and that connection with the side-face wiring (conductor 5b) and rewiring layer (conductor 5a) is attained by contact on a flat surface. Thus, when a side face has wiring with which electrical installation is attained by superficial contact, a semiconductor chip can be designed, without being restrained as usual, without spoiling the dependability of electric connection. Furthermore, any number of steps of this semiconductor device can be easily piled up by forming a solder ball in external terminal 7a like this example, and connecting with external terminal 7b of other semiconductor devices.

[0012] Drawing 2 - drawing 4 are the sectional views showing the manufacture approach of the 1st example of this invention in order of a process. First, on the wafer 8 covered with insulator 6e which has the electrode 3 made from aluminum and has opening on an electrode 3, and which is the passivation film, Ti/TiN which serves as barrier metal by the spatter is deposited, Au is deposited on it and plating substrate layer 4a is formed [drawing 2 (a)]. Next, the plating resist film 12 which has opening of the same pattern as the passivation film on a semi-conductor wafer (insulator 6e) is formed by the photolithography method [drawing 2 (b)]. Next, about 50 micrometers of Au(s) are deposited with electrolysis plating, a bump 4 is formed, and exfoliation removal of the plating resist film 12 is carried out after that [drawing 2 (c)].

[0013] Next, etching removal of the unnecessary plating substrate layer 3a is carried out by using the bump 4 as a mask, and insulator 6b is deposited all over after that. In addition, suppose that plating substrate layer 4a is included and shown to a bump 4, and insulator 6e is included in insulator 6b, and it is shown in subsequent displays [drawing 2 (d)]. Next, flattening is ground and carried out until a bump's 4 front face exposes the insulator 6b by the CMP method. After forming the plating resist film 13 on it furthermore, plating activation is performed, a catalyst bed is formed in the whole surface, and only the catalyst bed on the plating resist film 13 is removed. and an electroless deposition method -- Cu -- 20 micrometers -- depositing -- a conductor -- 5a is formed. The rewiring layer 11 is formed of the above [drawing 2 (e)]. Next, exfoliation removal of the plating resist film 13 is carried out, 50 micrometers of solder resists are deposited all over the, insulator 6a is formed, and patterning of the resist mask 14 is carried out on it [drawing 2 (f)].

[0014] Next, dry etching removes insulator 6a on an external electrode formation field by using the resist mask 14 as a mask [drawing 3 (g)]. In addition, it may be made to perform the process of etching of this insulator 6a in the case of the process of next drawing 4 (l). Next, a slot 9 is formed in order to cut this to a semiconductor chip 2. the cutting depth -- the conductor of the rewiring layer 11 -- it carried out to to this side of 5a, and the place whose insulator 6b is lost completely. The condition was set to the blade thickness of 300 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm at cutting using dicing equipment. Moreover, infrared radiation was used for positioning of cutting of the direction of a flat surface at this time. Since infrared radiation had the property which penetrates silicon, it carried out the image processing of the aluminum recognition mark on the front face of a semiconductor chip (not shown), read it, and was positioned.

[0015] the depth of cutting -- perfect -- insulator 6b -- losing -- and a conductor -- it is necessary to control 5a in the depth to leave Wear of the mechanical precision of the depth direction of dicing

equipment and a blade and member thickness dispersion are thought as an error of the depth direction. The mechanical precision of equipment is 0.5 micrometers. Moreover, if the wear of some lines of a blade is cut and offset will be applied on the way, it is cancellable. cutting dispersion in member thickness -- a conductor -- what is necessary is to take into consideration only thickness dispersion of insulator 6a which is below it, since it is to this side of 5a Since it is only one layer of insulator 6this time, it is stopped by about 2 micrometers. Therefore, it is about total 2.5micrometer, and since grinding of the five ais only deeply carried out about 2.5 micrometers of conductors even if it cuts by expecting this, it is satisfactory. performing grinding, when a rewiring layer turns into a multilayer **** -- a conductor -- [drawing 3 (h)] which needs the device of thickening thickness of 5a.

[0016] Next, skiing JINGU of the epoxy resin of optimum dose was applied and carried out on the wafer 8 cut top face, it embedded in the slot 9, and insulator 6c was formed in the wafer top face and the slot 9. And 150-degree-C heat treatment of 1 hour is performed, and insulator 6c is stiffened [drawing 3 (i)]. Next, a through hole 10 is formed in the predetermined part of embedded insulator 6c. Laser was used for this through hole formation. a through hole 10 -- insulator 6c -- forming -- a conductor -- although 5a must not be penetrated, since it is possible to delete by the laser output with the weaker insulator in an insulator and a conductor -- [drawing 3 (j)] with an easy setup of laser radiation conditions.

[0017] next, the plating substrate layer which consists of Ti/TiN and Cu by the spatter -- forming -- a conductor -- the electrolytic plating after forming the plating resist film which has opening on a formation field -- Cu -- depositing -- a through hole 10 wall, base, and insulator 6c top -- a conductor -- 5b is formed. thereby -- an electrode 3, a bump 4, conductor 5a, and a conductor -- 5b is connected electrically. Next, the plating resist film is removed and etching removal of the exposed plating substrate layer is carried out [drawing 4 (k)]. 6d of next, insulators which are a solder resist -- forming -- alternative -- opening -- carrying out -- a conductor -- [drawing 4 (l)] which exposes 5b and forms external terminal 7b. Then, external terminal 7a is formed. Other solder may be used although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a. Moreover, nothing may not be like external terminal 7b [drawing 4 (m)]. . At the end, it cuts and a semiconductor device 1 is obtained. Dicing equipment was used for cutting. Dicing conditions were set to the blade thickness of 50 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm [drawing 4 (n)].

[0018] Drawing 5 is the sectional view of the semiconductor device 1 of the 2nd example of this invention. the same reference number should give a part equivalent to the part of the example shown in drawing 1 in drawing 5 -- the explanation which overlaps in that of ********** is omitted. this example -- setting -- the conductor of the side face of a semiconductor device 1 -- external electrode 7c is prepared in 5b. Thereby, the further high density assembly becomes possible. Moreover, the manufacture approach of this semiconductor device 1 is the same as the manufacture approach of the semiconductor device 1 of drawing 1 , and after the cutting process shown in drawing 4 (n) is completed, it is acquired by laser's etc. removing 6d of some insulators, and preparing external electrode 7c.

[0019] As stated above, the description of the manufacture approach of the semiconductor device of this invention is that it can carry out wafer batch processing in spite of [drawing 3 (h)] cut once, in order to form wiring of a side face, after performing rewiring in the state of a wafer. Since the rewiring layer is supporting the semiconductor chip even if it cuts a wafer, positioning at each process is easy. Moreover, a man day can also be reduced for batch processing.

[0020] As mentioned above, although the desirable example of this invention was explained, proper modification is possible for this invention within limits which are not limited to these examples and do not deviate from the summary of this invention. For example, although a bump's formation approach was performed with electrolysis plating, you may form with the bonding method, vacuum deposition, or a replica method. moreover, the conductor same in the example -- although the external terminals 7b and 7c were formed on 5b, you may make it not form other external terminals in conductor 5b in which external terminal 7c was formed Moreover, in the example, all external terminals may prepare the external terminal mutually connected by Conductors 5a and 5b, without connecting with an electrode if

needed, although it connects with the electrode 3 of a semiconductor chip.

[Translation done.]